

5-in-1 Ethernet Package

The 5-in-1 Ethernet Package includes the following components:

emBetter TCP/IP-Protocol-Suite

- ported to Altera NIOSII embedded processor
- direct support of Ethernet MAC components
- delivered with source code
- extensive documentation
- supported protocols for connectivity
 - ARP, ICMP, IP, UDP, TCP, DHCP, DNS
- server & client applications
 - HTTP server, SMTP client, TFTP server
- drivers for the following PHYs
 - AMD: 79C874 NetPHY
 - Broadcom: BCM 5201
 - National Semi.: DP83847, DP83865
- other drivers can easily be included

Ethernet MAC

- Altera Avalon bus interfaces
 - slave interface for data management
 - master interface (DMA) for data transfer
- 10/100 Mbit/sec full/half-duplex
- delivered with Verilog source code
- extensive documentation

hardware:

The DBGIG1 module is a physical layer daughter card equipped with a Santa Cruz header, designed for the Altera Nios Development Boards. It provides a 10/100/1000 MBit/s physical interface for the use of an FPGA-integrated MAC.

The module is equipped with the National Semiconductor DP83865 GigPHYTER.

reference designs

- Altera: NiosII Development Kit Cyclone Edition
- Altera: NiosII Development Kit StratixII Edition
- EBV: DB1C12 Cyclone Evaluation Board

Contact



Steinbeis-Transferzentrum Embedded Design
und Networking an der Berufsakademie Lörrach
Prof. Dr.-Ing. Axel Sikora
Dipl.-Ing. Dipl.-Wirt.-Ing.

Hangstraße 46-50
79539 Lörrach
GERMANY

Phone: (+49) 76 21 / 20 71-441
Fax: (+49) 76 21 / 20 71-495
Website: www.stzedn.de
E-Mail: sikora@ba-loerrach.de



MaCo-Engineering

Dipl.-Ing. Marc Colling
Schlossstrasse 50
66352 Karlsbrunn
GERMANY

Phone: (+49) 68 09 / 70 20 190
Fax: (+49) 68 09 / 70 20 191
Website: www.MaCo-Engineering.de
E-Mail: Marc.Colling@MaCo-Engineering.de



STEINBEIS-TRANSFERZENTRUM
EMBEDDED DESIGN
UND NETWORKING
(STZEDN)



MaCo-Engineering

5-in-1 Ethernet Package

including

TCP/IP-
Protocol-Suite
+
10/100 Ethernet
MAC
+
10/100/1000
PHY Card

Introduction

With the Internet offering high performance and reliable data exchange, an added value to products can be achieved by adding Internet connectivity:

- global availability
- proven protocols
- redundant infrastructure and
- low cost per node
- system independent connectivity

A large number of Internet nodes use Ethernet for their connectivity. Nearly 30 years after its invention, Ethernet is still gaining popularity in two ways: It is not only the improvements to Ethernet for higher data rates, but many extensions for its industrial applicability. In addition, all newly sold computers are equipped with Ethernet. As a result Ethernet is widely spread.

The main advantages of Ethernet are

- high data throughput
- overwhelming compatibility
- low cost components
- persistent connectivity

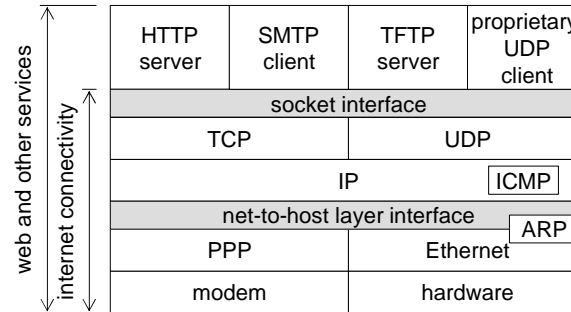
The broad applicability of Ethernet leads to the necessity to provide solutions for high performance embedded Ethernet. The main advantage comes with the close hardware-software-co-design, enabling flexibility and performance. While major parts of the communication stack are kept in software, computing intense portions are performed in hardware on the chip.

The “5-in-1 Ethernet Package” brings high performance Ethernet to embedded systems on five levels:

application	HTTP, ...	emBetter TCP/IP Stack for NIOS II
transport	TCP or UDP	
network	IP	
media access	Ethernet MAC as synthesizable RTL core	
physical level	PHY Card	

emBetter – Protocol Suite

The TCP/IP protocol suite is a modular system. It offers through this the complete protocol stack from user interface down to the physical layer out of one hand. The development further server or client applications is easily possible through the Berkeley-Socket-Interface (init, open, close, read, write).



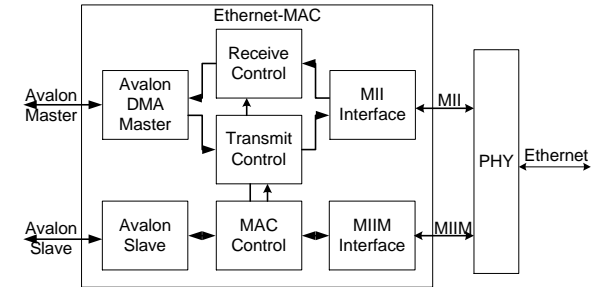
The use of pure ANSI-C and a minimum of external library functions make the emBetter protocol suite highly portable to a variety of compilers and microcontrollers. Hardware related functions are contained in one single file, leading to a smooth design flow. Even single protocols or functions can be disabled at compile time to adapt the software to its desired functionality (e.g. ICMP, SMTP). Additionally the memory usage can be exactly adjusted to the resources available.

The emBetter protocol stack can be used with an OS or typically as standalone stack. It uses around 35kB of ROM and requires at least 4kB of RAM. For the best performance it can manage up to 100kB of RAM.

Very popular is the adaptation to the scalable Nios-Processor from Altera, that can be implemented in every Altera FPGA (Programmable Logic Device). In conjunction with the Nios processor the emBetter proves its scalability and efficiency. The use in the FPGA allows high data transfer rates of up to 4.2 MByte / s (sustained, NIOSI processor with 50 MHz clock).

Ethernet MAC

The 10/100 Media Access Controller (MAC) consists of synthesizable Verilog RTL core that provides all features necessary to implement the Layer 2 protocol of the Ethernet standard. It is designed to run according to the IEEE 802.3 and 802.3u specifications that define the 10 Mbps and 100 Mbps Ethernet standards, respectively.



The MAC cares among other things about flow control, the automatic generation of control frames in full duplex mode (IEEE 802.3x), collision detection and auto re-transmission on collisions in half duplex mode (CSMA/CD protocol), as well as the 32-bit CRC generation/checking and the preamble generation and removal.

To gain performance on one hand and easy processor control on the other hand the MAC has two 32-bit Avalon bus interfaces. Through the slave interface the Nios processor can manage the whole functionality of the MAC and the connected PHY, whereas the DMA-capable master interface is used by the MAC to read/write the data streams to memory independent of the Nios processor.

In order to further increase the performance, up to 128 “Buffer Descriptors” can be used by the processor to inform the MAC where to read data from for a transmission or where to write data to for a reception.